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Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	09/832,867
				Filing Date	April 12, 2001
				First Named Inventor	Shunpei YAMAZAKI, et al.
				Group Art Unit	2822
				Examiner Name	Monica Lewis
Sheet	1	of	3	Attorney Docket Number	0756-2294

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U.S. PATENT DOCUMENTS						
Examiner Initials ¹	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
HL		4,963,504		Huang	10/16/90	
		5,323,042		Matsumoto	06/21/94	
		5,399,502		Friend et al.	03/21/95	
		5,412,240		Inoue et al.	05/02/95	
		5,532,175		Racanelli et al.	07/02/96	
		5,543,340		Lee	08/06/96	
		5,543,947		Mase et al.	08/06/96	
		5,583,067		Sanchez	12/10/96	
		5,581,092		Takemura	12/03/96	
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		6,166,397		Yamazaki et al.	12/26/00	
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		6,211,536		Zhang	04/03/01	
		6,259,138		Ohtani et al.	07/10/01	
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Page 1	2	of	3	Attorney Docket Number	0756-2294

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SL		6,281,552		Kawasaki et al.	08/28/01	
		6,284,577		Suzawa et al.	09/04/01	
		6,303,963		Ohtani et al.	10/16/01	
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ³
SL		US Patent Application Serial No. 10/386,257 including specification, drawings, claims, and filing receipt; filed March 11, 2003; Inventor: Hideto Ohnuma.	
		US Patent Application Serial No. 09/454,146 including specification, drawings, claims, and filing receipt; filed December 3, 1999; Inventors: Shunpei YAMAZAKI, et al.	
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		Hwang et al., "High Performance Submicron SOI/CMOS with an Elevated Source/Drain Structure," PROCEEDINGS OF THE ANNUAL SOS/SOI TECHNOLOGY CONFERENCE, IEEE, Vol. 19, 1993, pp. 132-133.	ENG
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Sheet 3	of 3		

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		Office ³	Number ⁴	Kind Code ⁵ (if known)				
SLC		JP	04-369271		Takeda et al.	12/22/92		FULL
		JP	05-102483		Ueda	04/23/93		FULL
		JP	06-037314		Tsuchimoto	02/10/94		AB
		JP	07-202210		Taniguchi	08/04/95		AB
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		EP	0 803 911		Adan et al.	10/29/97		ENG
SLC		JP	10-135468		Yamazaki et al.	05/22/98		AB

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
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SLC		Tanaka, et al., "Ultrafast Operation of V _{th} -Adjusted p ⁺ -n ⁺ Double-Gate SOI MOSFET'S," IEEE Electron Device Letters, Vol. 15 (Oct., 1994), No. 10, pp. 386-388.	ENG
		Inui et al., "Thresholdless Antiferroelectricity in Liquid Crystals and its Application to Displays," J. Mater Chem., 1996, 6(4), pp. 671-673.	ENG
		Takada, et al., PROCEEDINGS OF 46 TH SPRING MEETINGS OF THE SOCIETY FOR APPLIED PHYSICS OF JAPAN, 28P-V-8, page 1316.	NONE
		Hwang et al., "Novel Polysilicon/TiN Stacked-Gate Structure for Fully-Depleted SOI/CMOS," IEDM '92, pp. 345-348.	ENG
		Yoshihara, EKISHO, Vol. 3, No. 3, pp. 190-194.	NONE
		Furue et al., "P-78: Characteristics and Driving Scheme of Polymer-Stabilized Monostable FLCD Exhibiting Fast Response Time and High Contrast Ratio with Gray-Scale Capability," SID '98 DIGEST, pp. 782-785.	ENG
SLC		Hatano et al., "A Novel Self-Aligned Gate-Overlapped LDD Poly-Si TFT with High Reliability and Performance," IEDM '97, pp. 523-526.	ENG

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